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From SPICE Netlist to Allegro Design Sub-circuit

Introduction

Intersil provides a SPICE model for all our new precision Opamps. The SPICE model netlist is included in the data sheet, along with simulation vs characterization curves. Reference application note AN1556 for details on the making of the SPICE models.

This application note will walk the user through the process of taking the netlist from the data sheet and creating a sub-circuit to drop into a Cadence Allegro Design simulator.

Copying the SPICE Netlist

Download the Intersil data sheet from the web. The data sheet will be in pdf format. Open the pdf document and right click to enable the select tool, if it is not already selected (Figure 1). This will enable you to then copy and paste the entire netlist

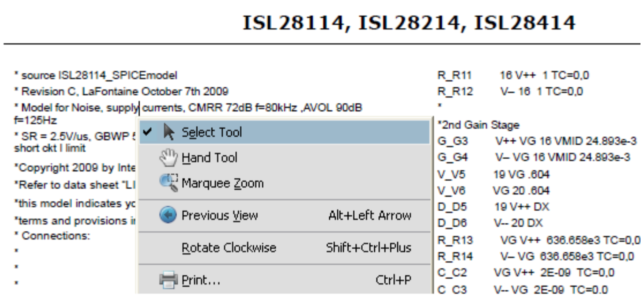


FIGURE 1. TURN ON THE SELECT TOOL IN THE PDF DATA SHEET

into notepad. Scroll towards the end of the data sheet and find the SPICE netlist (Figure 3) and copy it into notepad. Name the file with the extension **.MOD** (not case sensitive) as shown in Figure 2. This file needs to be saved in a common directory with all the other SPICE files for this design.

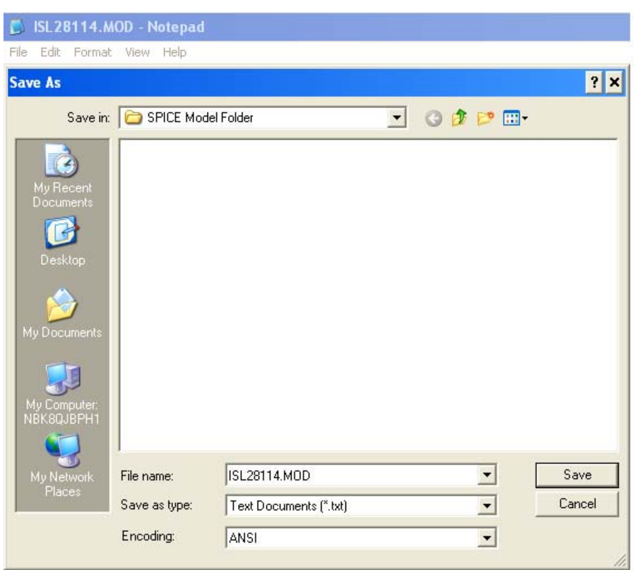
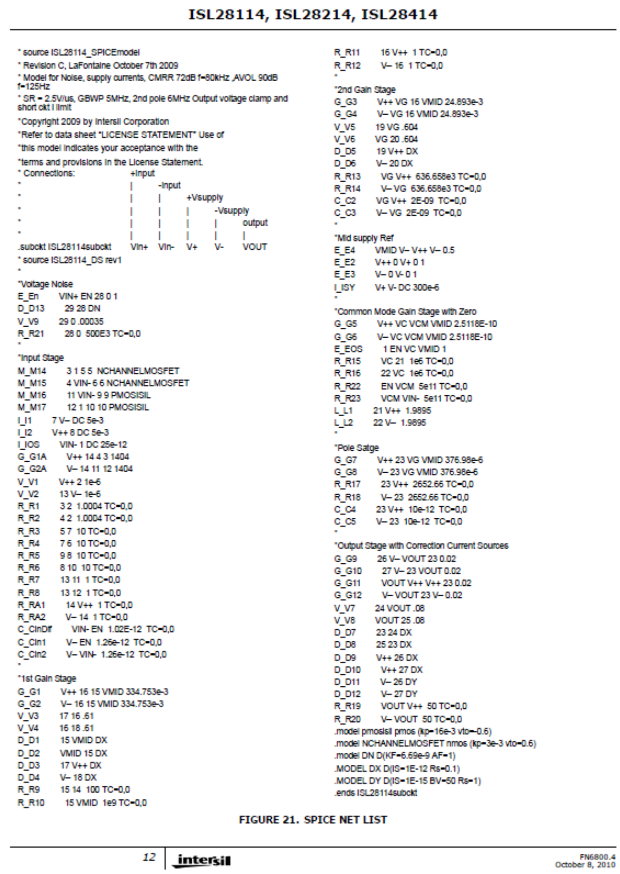


FIGURE 2. SAVING NOTE PAD FILE AS .MOD


ISL28114, ISL28214, ISL28414

```
* source ISL28114_SPICEmodel
* Revision C, LaFontaine October 7th 2009
* Model for Noise, supply currents, CMRR 72dB f=80kHz ,AVOL 90dB
f=125Hz
* SR = 2.5V/us, GBWP 5MHz, 2nd pole 6MHz Output voltage clamp and
short ckt I limit
*Copyright 2009 by Intersil Corporation
*Refer to data sheet "LICENSE STATEMENT" Use of
*this model indicates your acceptance with the
*terms and provisions in the License Statement.
* Connections:          +input
*                       |     -input
*                       |     |     +Vsupply
*                       |     |     |     -Vsupply
*                       |     |     |     |     output
*                       |     |     |     |     |
.subckt ISL28114subckt  Vin+  Vin-  V+    V-    VOUT
* source ISL28114_DS rev1
*
*Voltage Noise
E_En     VIN+ EN 28 0 1
D_D13    29 28 DN
V_V9     29 0 .00035
R_R21    28 0  500E3 TC=0,0
*
*Input Stage
M_M14    3 1 5 5  NCHANNELMOSFET
M_M15    4 VIN- 6 6 NCHANNELMOSFET
M_M16    11 VIN- 9 9 PMOSISIL
M_M17    12 1 10 10 PMOSISIL
I_I1     7 V– DC 5e-3
I_I2     V++ 8 DC 5e-3
I_IOS    VIN- 1 DC 25e-12
G_G1A    V++ 14 4 3 1404
G_G2A    V– 14 11 12 1404
V_V1     V++ 2 1e-6
V_V2     13 V– 1e-6
R_R1     3 2  1.0004 TC=0,0
R_R2     4 2  1.0004 TC=0,0
R_R3     5 7  10 TC=0,0
R_R4     7 6  10 TC=0,0
R_R5     9 8  10 TC=0,0
R_R6     8 10  10 TC=0,0
R_R7     13 11  1 TC=0,0
R_R8     13 12  1 TC=0,0
R_RA1    14 V++  1 TC=0,0
R_RA2    V– 14  1 TC=0,0
C_CinDif VIN- EN  1.02E-12  TC=0,0
C_Cin1   V– EN  1.26e-12  TC=0,0
C_Cin2   V– VIN-  1.26e-12  TC=0,0
*
*1st Gain Stage
G_G1     V++ 16 15 VMID 334.753e-3
G_G2     V– 16 15 VMID 334.753e-3
V_V3     17 16 .61
V_V4     16 18 .61
D_D1     15 VMID DX
D_D2     VMID 15 DX
D_D3     17 V++ DX
D_D4     V– 18 DX
R_R9     15 14  100 TC=0,0
R_R10    15 VMID  1e9 TC=0,0
R_R11    16 V++  1 TC=0,0
R_R12    V– 16  1 TC=0,0
*
*2nd Gain Stage
G_G3     V++ VG 16 VMID 24.893e-3
G_G4     V– VG 16 VMID 24.893e-3
V_V5     19 VG .604
V_V6     VG 20 .604
D_D5     19 V++ DX
D_D6     V– 20 DX
R_R13    VG V++  636.658e3 TC=0,0
R_R14    V– VG  636.658e3 TC=0,0
C_C2     VG V++  2E-09  TC=0,0
C_C3     V– VG  2E-09  TC=0,0
*
*Mid supply Ref
E_E4     VMID V– V++ V– 0.5
E_E2     V++ 0 V+ 0 1
E_E3     V– 0 V- 0 1
I_ISY    V+ V- DC 300e-6
*
*Common Mode Gain Stage with Zero
G_G5     V++ VC VCM VMID 2.5118E-10
G_G6     V– VC VCM VMID 2.5118E-10
E_EOS    1 EN VC VMID 1
R_R15    VC 21  1e6 TC=0,0
R_R16    22 VC  1e6 TC=0,0
R_R22    EN VCM  5e11 TC=0,0
R_R23    VCM VIN-  5e11 TC=0,0
L_L1     21 V++  1.9895
L_L2     22 V–  1.9895
*
*Pole Satge
G_G7     V++ 23 VG VMID 376.98e-6
G_G8     V– 23 VG VMID 376.98e-6
R_R17    23 V++  2652.66 TC=0,0
R_R18    V– 23  2652.66 TC=0,0
C_C4     23 V++  10e-12  TC=0,0
C_C5     V– 23  10e-12  TC=0,0
*
*Output Stage with Correction Current Sources
G_G9     26 V– VOUT 23 0.02
G_G10    27 V– 23 VOUT 0.02
G_G11    VOUT V++ V++ 23 0.02
G_G12    V– VOUT 23 V– 0.02
V_V7     24 VOUT .08
V_V8     VOUT 25 .08
D_D7     23 24 DX
D_D8     25 23 DX
D_D9     V++ 26 DX
D_D10    V++ 27 DX
D_D11    V– 26 DY
D_D12    V– 27 DY
R_R19    VOUT V++  50 TC=0,0
R_R20    V– VOUT  50 TC=0,0
.model pmosisil pmos (kp=16e-3 vto=-0.6)
.model NCHANNELMOSFET nmos (kp=3e-3 vto=0.6)
.model DN D(KF=6.69e-9 AF=1)
.MODEL DX D(IS=1E-12 Rs=0.1)
.MODEL DY D(IS=1E-15 BV=50 Rs=1)
.ends ISL28114subckt
```

FIGURE 21. SPICE NET LIST

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FIGURE 3. NETLIST FROM DATA SHEET

Model Editor

Open the Cadence model editor via the path shown in Figure 4 (Cadence SPB 16.2\AMS Simulator\Simulation Accessories\Model Editor) Note: This apnote is written using the SPB16.2 software. The look and feel may change with different revisions of the Cadence software, but the procedure will be the same.

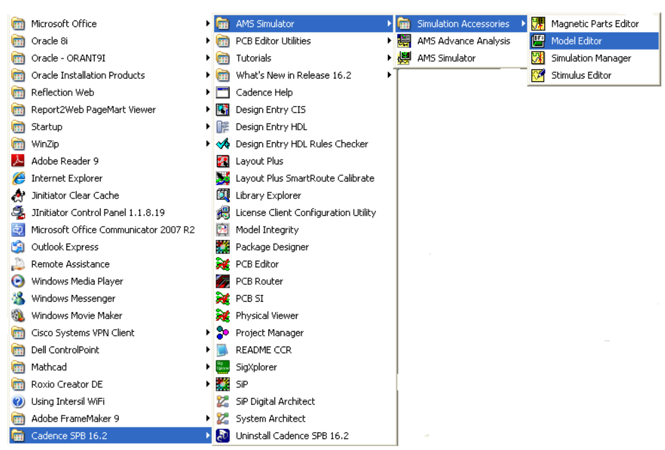

FIGURE 4. PATH TO CADENCE MODEL EDITOR

After selecting the Model Editor, the screen in Figure 5 will open up. Select Capture and click DONE.

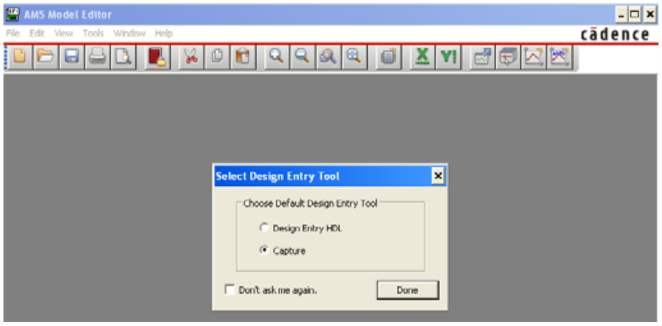

FIGURE 5. SELECT DESIGN ENTRY TOOL

Click on File in the tool bar and select New. Figure 6 will appear.

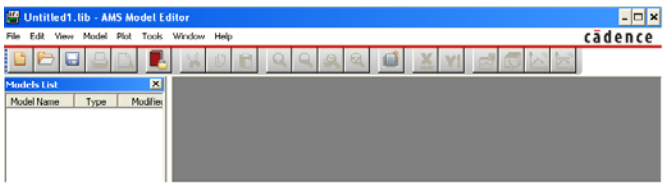

FIGURE 6. BEGINNING OF NEW MODEL

Click on Model in the tool bar and select Import. Then browse to the folder where you put the .MOD file. Figure 7 will appear. Select the desired .MOD file and click Open.

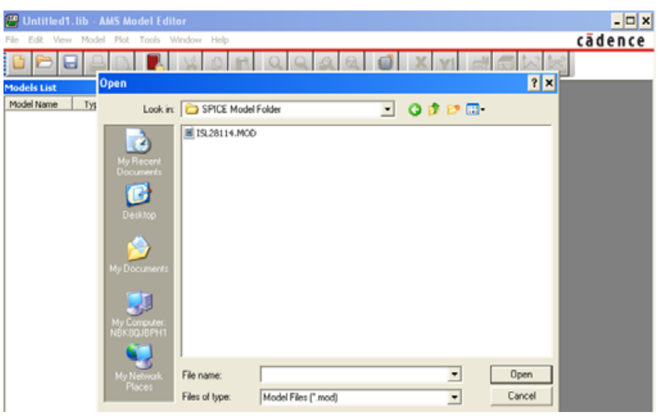

FIGURE 7. SELECT .MOD NETLIST

This will load the netlist into the Model editor tool as shown in Figure 8.

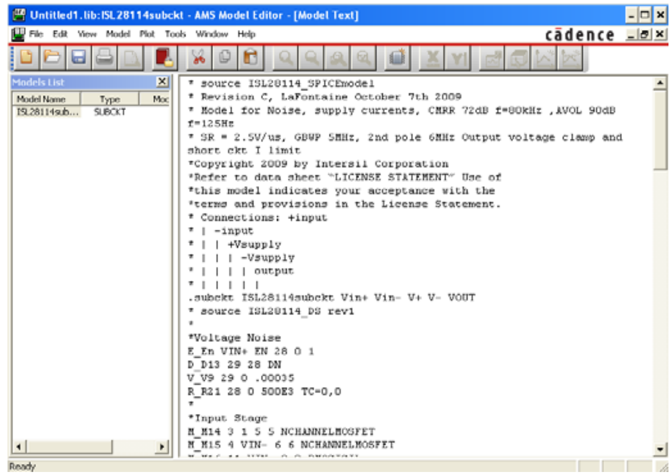

FIGURE 8. NETLIST LOADED INTO MODEL EDITOR

Click on File in the tool bar and select Save As. Then type the part name as the file name in Figure 9 and click Save. The file with the complete netlist is now saved as a .lib library file.

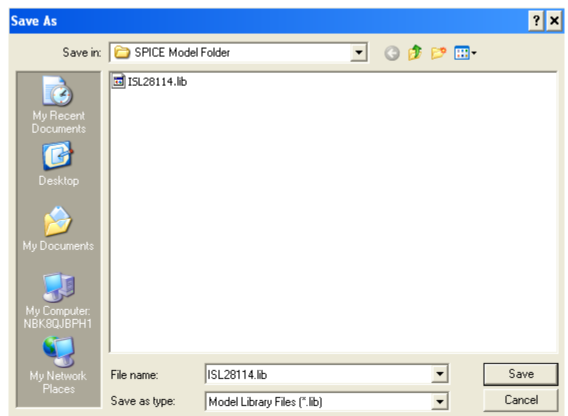

FIGURE 9. FILE SAVED AS .lib

Click on File in the tool bar and select Export to Capture Part Library. The Input Model Library path and the Output Part Library path will automatically be loaded as shown in Figure 10.

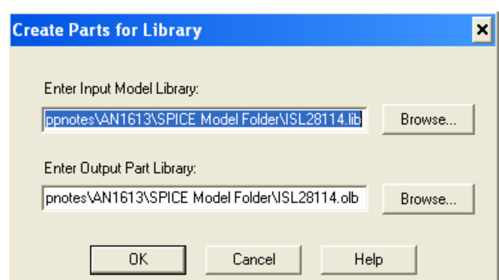

FIGURE 10. LIBRARY CREATION

Verify that the files paths are the same with the only difference being the .lib and .olb extensions.

Click OK and verify no Error messages or Warning messages as shown in Figure 11. Click OK.

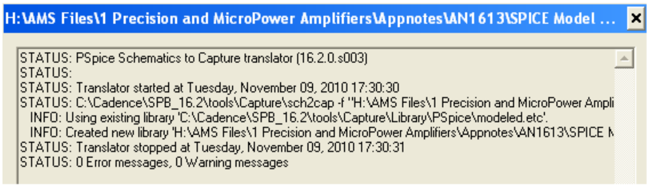

FIGURE 11. SCHEMATIC TO CAPTURE TRANSLATOR CHECK

Click on File in the tool bar and select Import Wizard [Capture]. Like before, both path names will load automatically and should have the same file paths with the only difference being the .lib and .olb extensions as shown in Figure 12.

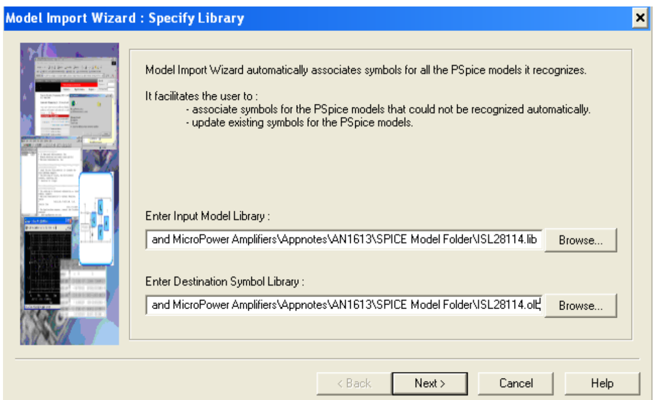

FIGURE 12. ASSOCIATE SYMBOL WITH SPICE MODEL

Click Next and the screen shown in Figure 13 will appear. This is the screen in which we will associate the pins of our SPICE model to the pins of the sub-circuit model. The symbol shown is a generic 5 pin device. We want our Opamp symbol to look like an Opamp. To do this click on the Replace Symbol button and select from the list of symbols provided with the Cadence program. This list is located at the following location on your C drive. C:\Cadence\SPB.16.2\tools\capture\libary\OPAmp.olb

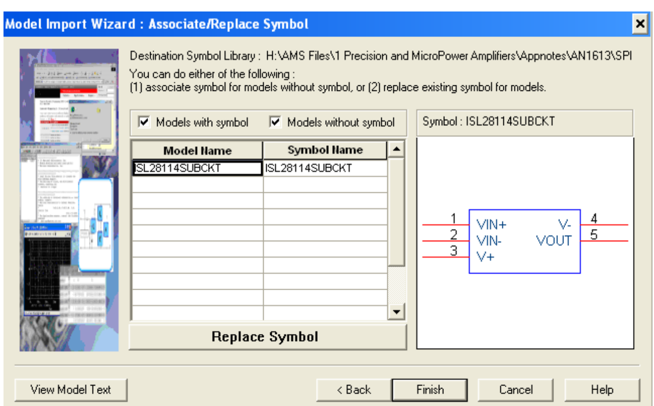

FIGURE 13. REPLACE GENERIC SYMBOL

If the location of your Cadence software was loaded in a different location, then search for Cadence\SPB.

When selecting your symbol, all that matters is the pin count. The numbers assigned to the symbol pins can be changed later. Just scroll through the list to find a symbol that matches a desired pinout and pin count of your device. In this example, we selected the TLC2201. Click Next.

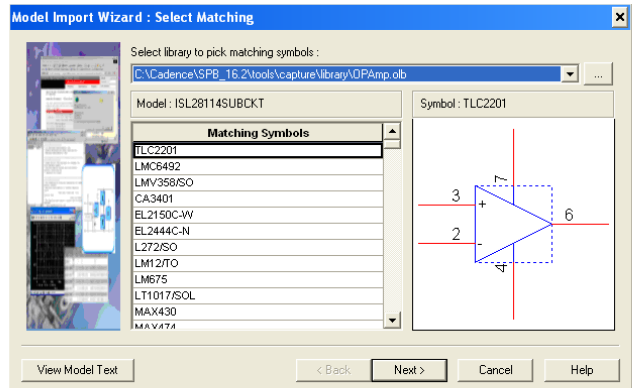

FIGURE 14. ASSOCIATE OP AMP SYMBOL WITH MODEL

Then click on the row under the Symbol Pin column to activate pull down menu box under the symbol column. Now pick the associated pin to match the Model Terminal function in the model terminal column. As shown in Figure 15.

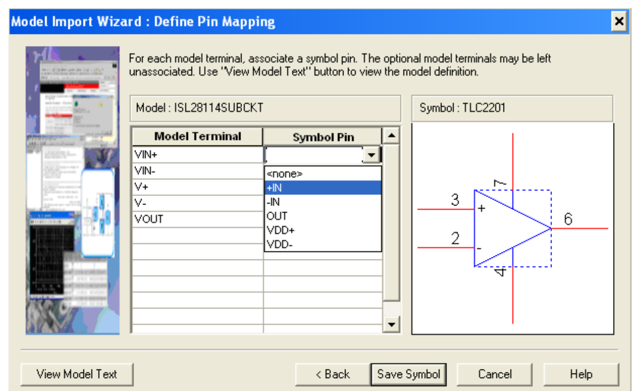

FIGURE 15. DEFINE PINS OF SYMBOL TO PINS OF MODEL

Repeat for all Model Terminal pins as shown in Figure 16.

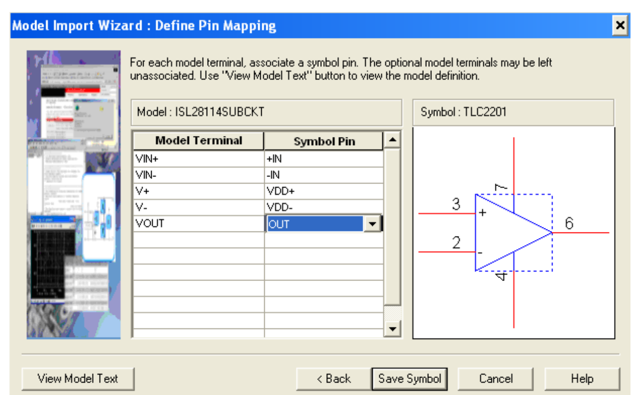

FIGURE 16. ALL PINS ASSOCIATED TO SYMBOL

Click Save Symbol and Figure 17 will appear. Verify no Error messages or Warning messages. Click OK and then close the Model Editor.

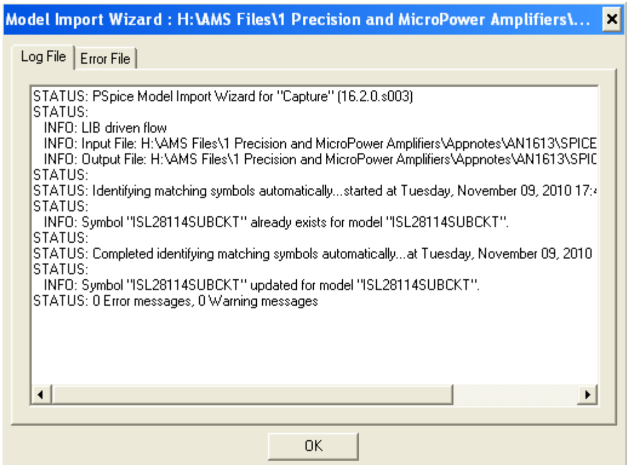

FIGURE 17. MODEL IMPORT WIZARD CHECK

Using the New Sub-circuit to Run Simulations

Open the Cadence Software. Figure 18 shows the path to select the Design Entry CIS.

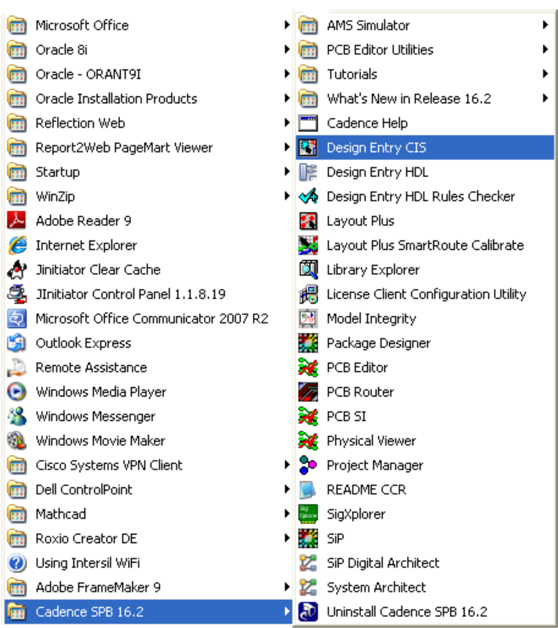

FIGURE 18. PATH TO DESIGN ENTRY CIS

Figure 19 shows the Cadence Product Choices. Select Allegro Design Entry CIS and Click OK.

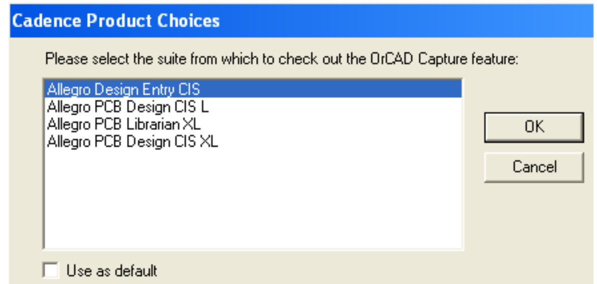

FIGURE 19. CADENCE PRODUCT CHOICES

Click on File in the tool bar and select New, and then Project. The screen shown in Figure 20 will appear. Type in the name of the project and select Analog of Mixed A/D button. Browse to where you saved the Netlist in the common directory (you must have all the files located in the same directory) and click OK.

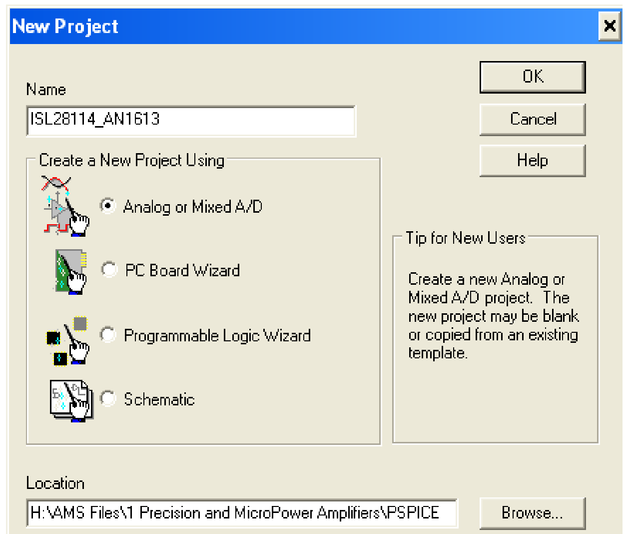

FIGURE 20. SCREEN TO SETUP NEW PROJECT

The screen shown in Figure 21 will appear. The user can select to base their new project on an existing project or start a new one. Selecting to base upon an existing project will carry over the existing project with all the simulation profiles and schematics. This can be a real time saver if the new project is very similar to an old project. In this example, we will chose to create a new project.

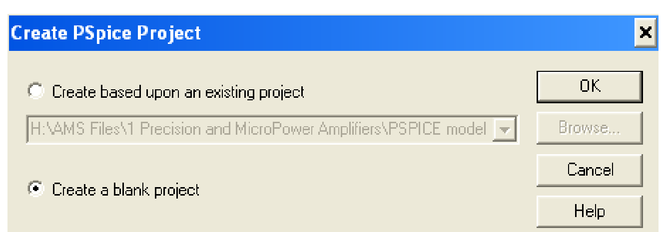

FIGURE 21. CREATING A NEW PROJECT OPTIONS

Click OK and the screen in Figure 22 will appear. Click on the SCHEMATIC1 to open the Page tab and then Click on the page tab to open the Schematic1 page. This is where the new sub-circuit will be placed to run the simulations.

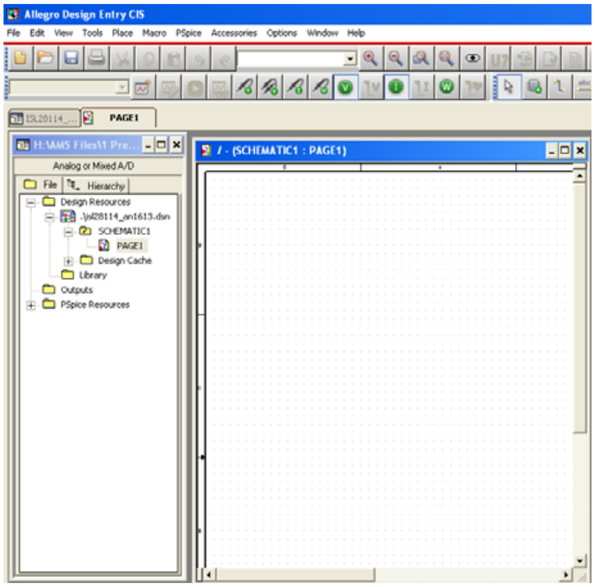

FIGURE 22. SIMULATION SCHEMATIC PAGE

Before we can place the new sub-circuit model and run a simulation, we need to set-up the simulation profile and add the library. Click on PSpice in the tool bar and select New Simulation Profile. Figure 23 will appear. Then type in any name that will help you keep track of the different simulations. Then click Create and Figure 24 will appear.

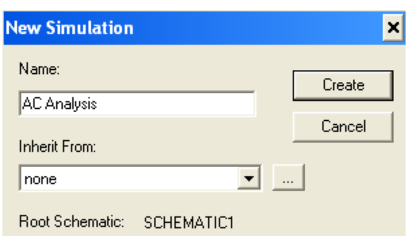

FIGURE 23. NAMING SIMULATION PROFILE

Click the Configuration Files tab. Then click on Library in the Category field (highlighted in blue). Browse to where to saved the Library file. Then click the Add to Design button. The Simulation Settings screen should look like that shown in Figure 24 with the file path name being the location of the common directory. Click the Apply button.

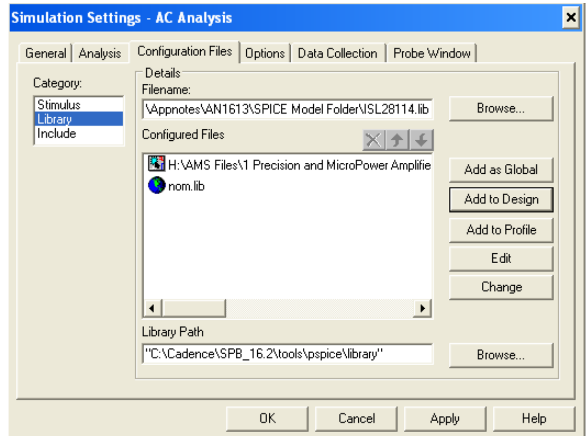

FIGURE 24. CONFIGURATION FILE TO ADD LIBRARY

Now click the analysis tab and configure the simulation as shown in Figure 25. The analysis selected for this example is an AC Sweep/Noise. Other types of analysis are: Time Domain (Transient), DC Sweep and Bias Point. Just click the down arrow in the analysis type section to access the different Analysis options. When done, click OK.

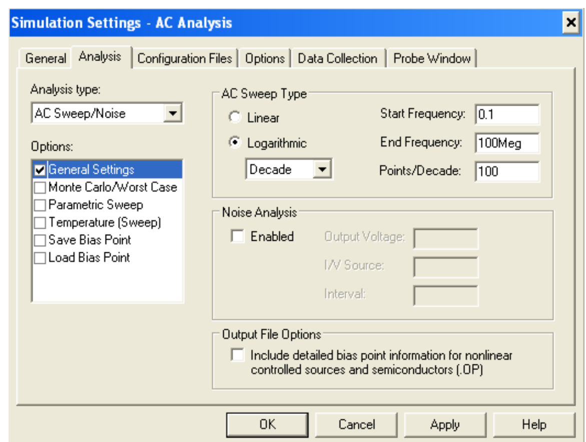

FIGURE 25. SCREEN TO SET-UP THE ANALYSIS PROFILE CONFIGURED

The user will need to add the Library .olb to the simulator. To do this, click on Place in the tool bar and select Part. This will bring up the part placement tool at the far right of the simulator as shown in Figure 26.

To add the library, click on the tab where the arrow is pointing to in Figure 26.

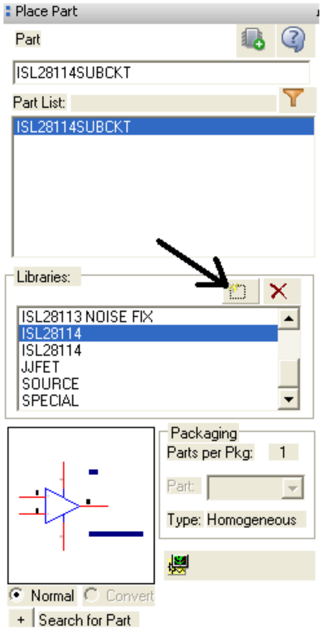

FIGURE 26. PART PLACEMENT TOOL

This will bring up the screen shown in Figure 27. Browse to where you saved the Netlist in the common directory and click Open.

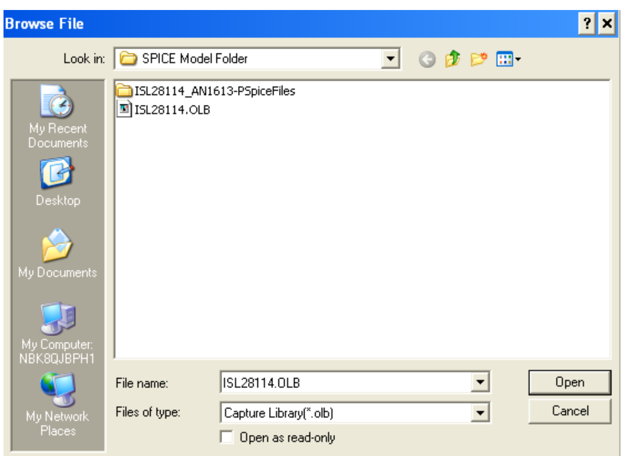

FIGURE 27. CONNECTING THE SYMBOL LIBRARY TO SIMULATOR

Now you are ready to add the sub-circuit to your simulation schematic and start your simulations.

Adding the Sub-circuit to Your Simulation Schematic

With the .lib file added to the simulation profile and the .olb file added to the Part placement tool, your are now ready to place the Opamp sub-circuit into your simulation schematic. Figure 28 shows the part placement tool after the .olb has been added to it. Under the Libraries section, find the new .olb symbol you added in the previous step (highlighted in blue). Double click on the file to add the sub-circuit to the Part list section (also highlighted in blue). Double click on the Part in the part list section to add the sub-circuit to the simulation schematic.

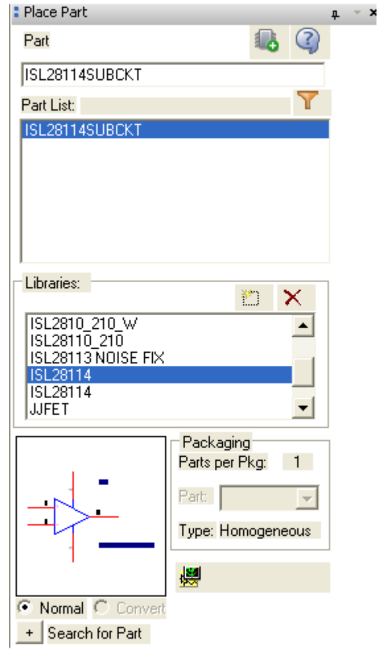

FIGURE 28. ADDING SUB-CIRCUIT TO SIMULATION SCHEMATIC

Figure 29 shows sub-circuit in a basic non-inverting application circuit. The simulation result showing AVOL (green trace) and Phase (pink) are shown in Figure 30.

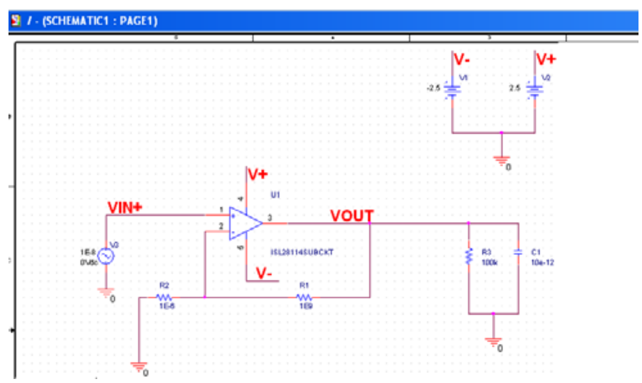

FIGURE 29. SIMULATION SCHEMATIC

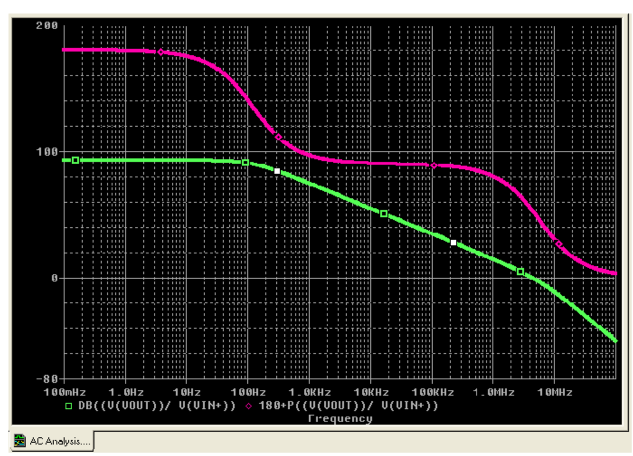

FIGURE 30. AVOL GAIN/PHASE SIMULATION RESULTS