Application Note 1613

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intersil

From SPICE Netlist to Allegro Design Sub-circuit

- VG 636.658e3 TC=0,0

? ×

VG V++ 2E-09 TC=0,0

V-- VG 2E-09 TC=0.0

Introduction

Intersil provides a SPICE model for all our new precision Opamps. The SPICE model netlist is included in the data sheet, along with simulation vs characterization curves. Reference application note AN1556 for details on the making of the SPICE models.

This application note will walk the user through the process of taking the netlist from the data sheet and creating a sub-circuit to drop into a Cadence Allegro Design simulator.

Copying the SPICE Netlist

📄 Print...

with all the other SPICE files for this design.

📋 ISL28114.MOD - Notepad

Save in: C SPICE Model Folde

File name

Encoding

Save as type

Save As

0

B

Download the Intersil data sheet from the web. The data sheet will be in pdf format. Open the pdf document and right click to enable the select tool, if it is not already selected (Figure 1). This will enable you to then copy and paste the entire netlist



FIGURE 1. TURN ON THE SELECT TOOL IN THE PDF DATA SHEET

into notepad. Scroll towards the end of the data sheet and find

the SPICE netlist (Figure 3) and copy it into notepad. Name the file with the extension .MOD (not case sensitive) as shown in

Figure 2. This file needs to be saved in a common directory

ISL28114, ISL28214, ISL28414

C_C2

C C3

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Save

Cancel

Ctrl+P

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FN6800.4 October 8, 2010

FIGURE 3. NETLIST FROM DATA SHEET

Model Editor

Open the Cadence model editor via the path shown in Figure 4 (Cadence SPB 16.2\AMS Simulator\Simulation Accessories\ Model Editor) Note: This apnote is written using the SPB16.2 software. The look and feel may change with different revisions of the Cadence software, but the procedure will be the same.

	Microsoft Office	۲	Control	AMS Simulator	►	ā	Simulation Accessories	1	Magnetic Parts Editor
	Oracle 8i	Þ	(m)	PCB Editor Utilities	•	ų.	AMS Advance Analysis	en	Model Editor
	Oracle - ORANT9I	•		Tutorials	►		AMS Simulator	28	Simulation Manager
	Oracle Installation Products	•	m	What's New in Release 16.2	×	Γ		2	Stimulus Editor
•	Reflection Web	•		Cadence Help				_	
	Report2Web PageMart Viewer	۲		Design Entry CIS					
	Startup	Þ	F	Design Entry HDL					
	WinZip	•	-	Design Entry HDL Rules Checker					
X	Adobe Reader 9		2	Layout Plus					
Ø	Internet Explorer		24	Layout Plus SmartRoute Calibrate					
æ	Jinitiator Clear Cache		۵Į	Library Explorer					
3	JInitiator Control Panel 1.1.8.19		遇	License Client Configuration Utility					
éę.	Microsoft Office Communicator 2007 R2		Ŕ	Model Integrity					
3	Outlook Express			Package Designer					
Þ	Remote Assistance		2	PCB Editor					
Θ	Windows Media Player		6	PCB Router					
12	Windows Messenger		24	PCB SI					
۹	Windows Movie Maker		26	Physical Viewer					
	Cisco Systems VPN Client	,	⊳	Project Manager					
	Dell ControlPoint	•		README CCR					
	Mathcad	۲	Rig Talanar	SigXplorer					
	Roxio Creator DE	۲		SIP					
0	Using Intersil WiFi		2	SiP Digital Architect					
	Adobe FrameMaker 9	,	2	System Architect					
G	Cadence SPB 16.2	Þ	Ð	Uninstall Cadence SPB 16.2					

FIGURE 4. PATH TO CADENCE MODEL EDITOR

ISL28114.MOD

ANSI

Text Documents (*.txt)

FIGURE 2. SAVING NOTE PAD FILE AS . MOD

ISL28114, ISL28214, ISL28414 source ISL28114_SPICEmo Revision C, LaFontaine Oct R_R11 R_R12 16 V++ 1 TC=0,0 V= 16 1 TC=0.0 Model for Noise, supply currents, CMRR 72dB 1-80kHz ,AVOL 90dB Stage V++ VG 16 VMID 24.893e-3 V-- VG 16 VMID 24.893e-3 19 VG 604 VG 20.604 19 V++ DX V-- 20 DX SR = 2.5V/us, GBWP 5MHz, 2nd pole 6MHz Output voltage clamp and short ckt | limit Copyright 2009 by Intersil Corporation 'Refer to data sheet "LICENSE STATEMENT" Use of "this model indicates your acceptance with the ms and provisions in the License Statem R_R13 R_R14 C_C2 C_C3 VG V++ 636.658e3 TC=0,0 V- VG 636.658e3 TC=0,0 VG V++ 2E-09 TC=0,0 V- VG 2E-09 TC=0,0 Ny Ref VMID V- V++ 1 V++ 0 V+ 0 1 V- 0 V- 0 1 V+ V- DC 300e subokt ISL28114s E_E4 E_E2 E_E3 source ISL28114_DS rev LISY Noise VIN+ EN 28 0 1 29 28 DN 29 0 .00035 28 0 500E3 TC=0,0 E_En D_D13 Wole can sage win 240 V++ VC VCM VMID 2.5118E-10 V - VC VCM VMID 2.5118E-10 1 EN VC VMID 1 VC 21 1e6 TC=0,0 22 VC 1e6 TC=0,0 V_V9 R_R21 3155 NC 3 15 5 NCHANEL 4 VIN-5 6 NCHANEL 11 VIN-9 5 MC031 12 1 10 10 MC031L VI+ 8 DC 5e-3 VIN-10 C28-12 VI+14 3 1404 V+14 11 12 1404 V+12 1e5 13 V-1e5 32 1.000 TC=0.0 75 10 TC=0.0 75 10 TC=0.0 75 10 TC=0.0 81 R_R22 R_R23 L_L1 L_L2 VCM VIN-21 V++ 1.98 22 V-EN VCM 5e11 TC-0,0 VCM VIN- 5e11 TC-0,0 "Pole 5 G_G7 G_G8 R_R17 R_R18 C_C4 C_C5 V+ 23 VG VMID 376.98e-V- 23 VG VMID 376.98e-23 V+ 2652.66 TC-0,0 V- 23 2652.66 TC-0,0 23 V++ 10e-12 TC-0,0 V- 23 10e-12 TC-0,0 *Output G_G9 G_G10 G_G11 G_G12 V_V7 V_V8 D_D7 D_D8 D_D9 D_D10 D_D11 D_D12 R_R19 26 V- VOUT 23 0.02 27 V- 23 VOUT 0.02 27 V- 23 VOUT 0.02 VOUT 14+ V- 23 0.02 V- VOUT 23 V- 0.02 24 VOUT .03 VOUT 25 .08 23 24 DX 25 23 DX V+ 25 DX V+ 25 DX V+ 25 DX V+ 25 DX V- 27 DX VOLT 23.0.0 14 V++ 1 TC=0,0 V- 14 1 TC=0,0 VIN- EN 1.02E-12 TC=0.0 V-EN 1.25e-12 TC-0,0 V-VIN- 1.25e-12 TC-0,0 "1st G V++ 16 15 VMID 334.753 G_G1 G_G2 V_V3 V_V4 D_D1 D_D2 D_D3 D_D4 R_R9 R_R10 V++ 16 15 VMID 334.753e-3 V-- 16 15 VMID 334.753e-3 17 16.61 16 18.61 15 VMID DX VMID 15 DX VMID 15 DX V-- 18 DX 15 14 100 TC=0,0 15 VMID 1e9 TC=0,0 VOUT V++ 50 TC=0,0 V- VOUT 50 TC=0,0 nosisi pmos (kp=16e-3 vto=0.6) CHANNELMOSFET mos (kp=3e-3 vtr N D(KF=6.69e-9 AF=1) MODEL DX D(IS-1E-12 Rs-0.1) MODEL DY D(IS-1E-15 BV-50 Rs-1) FIGURE 21. SPICE NET LIST

After selecting the Model Editor, the screen in Figure 5 will open up. Select Capture and click DONE.



FIGURE 5. SELECT DESIGN ENTRY TOOL

Click on File in the tool bar and select New. Figure 6 will appear.

🔐 Untitled1.lib - AMS Model Ed	itor	- 🗆 ×
File Edit Yew Model Plot Tools	Window Help	cādence
	X D E Q Q Q Q I Z	
Models List X Model Name Type Modilies		

FIGURE 6. BEGINNING OF NEW MODEL

Click on Model in the tool bar and select Import. Then browse to the folder where you put the .MOD file. Figure 7 will appear. Select the desired .MOD file and click Open.



FIGURE 7. SELECT .MOD NETLIST

This will load the netlist into the Model editor tool as shown in Figure 8.

File Edit View Model Plot Tool	s Window Help C	ādence	_ 0 1
🖻 🗁 🖴 🖻 尾		X	
Indefa Lut X.J Nodel Herre Type Max 92,3311 (s.b.m. S.BCAT	<pre>* source ISL20114_SPICEmodel * Revision C, LaFontaine Octoher 7th 2009 * Model for Noise, supply currents, CHER 72dD f=00kHz , f=158H * SK = 2.5V/us, GBUP SHHz, 2nd pole GHHz Output voltage short ekt I limit ropyright 2009 by Intersil Corporation *Refer to data sheet ~LICENSE STATEMENT" Use of *This model indicates your acceptance with the *terme and provisions in the License Statement. * Connections: +input * - HYsupply * - Vsupply * - Vsupply * -Vsupply * - Usupply * Joutput * juncht ISL20114_DS rev1 * voltage Noise E_n VINE X28 0 SOOES TC=0.0 * * thrus Stage M149 21 S 5 NCLADENTLEOSFET</pre>		1
	M M15 4 VIN- 6 6 NCHANNELMOSFET		

FIGURE 8. NETLIST LOADED INTO MODEL EDITOR

Click on File in the tool bar and select Save As. Then type the part name as the file name in Figure 9 and click Save. The file with the complete netlist is now saved as a .lib library file.

Save As					? ×
Save in:	SPICE Model	Folder	• 6	Þ 📂 🛄-	
My Recent Documents Desktop My Documents My Conguter My Conguter	■ I5L28114.lb				
- S					
My Network Places	File name:	ISL28114.lib			Save
	Save as type:	Model Library Files (*.lib)		_	Cancel

FIGURE 9. FILE SAVED AS .lib

Click on File in the tool bar and select Export to Capture Part Library. The Input Model Library path and the Output Part Library path will automatically be loaded as shown in Figure 10.

Create Parts for Library	×
Fata las Alfadal Dana	
Enter Input Model Library: ppnotes\AN1613\SPICE Model Folder\ISL28114.lib	Browse
Enter Output Part Library:	
pnotes\AN1613\SPICE Model Folder\ISL28114.olb	Browse
OK Cancel Help	_

FIGURE 10. LIBRARY CREATION

Verify that the files paths are the same with the only difference being the .lib and .olb extensions.

Click OK and verify no Error messages or Warning messages as shown in Figure 11. Click OK.



FIGURE 11. SCHEMATIC TO CAPTURE TRANSLATOR CHECK

Click on File in the tool bar and select Import Wizard [Capture]. Like before, both path names will load automatically and should have the same file paths with the only difference being the .lib and .olb extensions as shown in Figure 12.

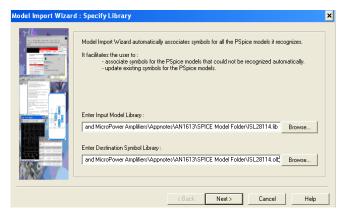


FIGURE 12. ASSOCIATE SYMBOL WITH SPICE MODEL

Click Next and the screen shown in Figure 13 will appear. This is the screen in which we will associate the pins of our SPICE model to the pins of the sub-circuit model. The symbol shown is a generic 5 pin device. We want our Opamp symbol to look like an Opamp. To do this click on the Replace Symbol button and select from the list of symbols provided with the Cadence program. This list is located at the following location on your C drive. C:\Cadence\SPB.16.2\tools\capture\libary\OPAmp.olb

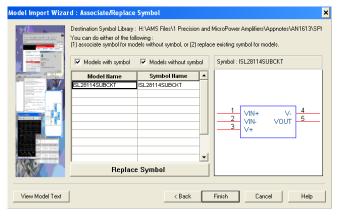


FIGURE 13. REPLACE GENERIC SYMBOL

If the location of your Cadence software was loaded in a different location, then search for Cadence $\SPB.$

When selecting your symbol, all that matters is the pin count. The numbers assigned to the symbol pins can be changed later. Just scroll through the list to find a symbol that matches a desired pinout and pin count of your device. In this example, we selected the TLC2201. Click Next.

r <u>11.</u>	Select library to pick matching symbols :	
	C:\Cadence\SPB_16.2\tools\capture\library\OPAmp	o.olb 💌 🗾 📖
And a second sec	Model : ISL28114SUBCKT	Symbol : TLC2201
and the second s	Matching Symbols	•
alasia-	TLC2201	
1000	LMC6492	
Concernence	LMV358/SO	1-
	CA3401	3 +
	EL2150C-W	6
11-1-1-1	EL2444C-N	2
	L272/SO	
A CONTRACTOR OF THE OWNER	LM12/TO	4
the second	LM675	-
10.0	LT1017/SOL	
NY A	MAX430	*
NO NOTA	MAV474	·

FIGURE 14. ASSOCIATE OP AMP SYMBOL WITH MODEL

Then click on the row under the Symbol Pin column to activate pull down menu box under the symbol column. Now pick the associated pin to match the Model Terminal function in the model terminal column. As shown in Figure 15.

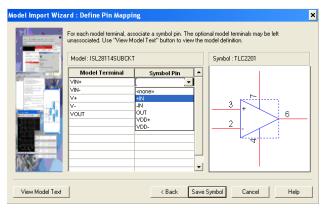


FIGURE 15. DEFINE PINS OF SYMBOL TO PINS OF MODEL

Repeat for all Model Terminal pins as shown in Figure 16.

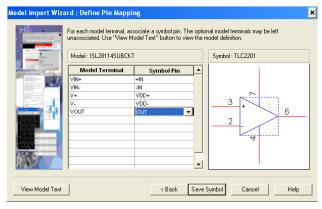


FIGURE 16. ALL PINS ASSOCIATED TO SYMBOL

Click Save Symbol and Figure 17 will appear. Verify no Error messages or Warning messages. Click OK and then close the Model Editor.

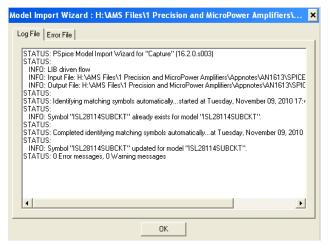


FIGURE 17. MODEL IMPORT WIZARD CHECK

Using the New Sub-circuit to Run Simulations

Open the Cadence Software. Figure 18 shows the path to select the Design Entry CIS.



FIGURE 18. PATH TO DESIGN ENTRY CIS

Figure 19 shows the Cadence Product Choices. Select Allegro Design Entry CIS and Click OK.

Please select the suite from which to check out the OrCAD Captu	re feature:
Allegro Design Entry CIS Allegro PCB Design CIS L Allegro PCB Librarian XL Allegro PCB Design CIS XL	OK Cancel
Use as default	

FIGURE 19. CADENCE PRODUCT CHOICES

Click on File in the tool bar and select New, and then Project. The screen shown in Figure 20 will appear. Type in the name of the project and select Analog of Mixed A/D button. Browse to where you saved the Netlist in the common directory (you must have all the files located in the same directory) and click OK.

New Project	×
Name ISL28114_AN1613	OK Cancel
Create a New Project Using Analog or Mixed A/D C PC Board Wizard C Programmable Logic Wizard C Schematic	Help Tip for New Users Create a new Analog or Mixed A/D project. The new project may be blank or copied from an existing template.
Location H:\AMS Files\1 Precision and MicroPower Amplifi	ers\PSPICE Browse

FIGURE 20. SCREEN TO SETUP NEW PROJECT

The screen shown in Figure 21 will appear. The user can select to base their new project on an existing project or start a new one. Selecting to base upon an existing project will carry over the existing project with all the simulation profiles and schematics. This can be a real time saver if the new project is very similar to an old project. In this example, we will chose to create a new project.

Create PSpice Project	×
C Create based upon an existing project	ОК
H:\AMS Files\1 Precision and MicroPower Amplifiers\PSPICE model	Browse
Create a blank project	Cancel
	Help

FIGURE 21. CREATING A NEW PROJECT OPTIONS

Click OK and the screen in Figure 22 will appear. Click on the SCHEMATIC1 to open the Page tab and then Click on the page tab to open the Schematic1 page. This is where the new sub-circuit will be placed to run the simulations.

Allegro Design Entry CIS		
File Edit View Tools Place Macro PSp	pice Accessories Options Window Help	
		3 8
I 🖉 🖾 🖓 (0 . 8 8 8 8 0 1 0 1 0 1 0 1 8 8	1 🛎
15120114 PAGE1		
👪 H:WMS Files\1 Pre 🗕 🗖 🗙	1 - (SCHEMATIC1 : PAGE1)	- 🗆 X
Analog or Mixed A/D		
File 4. Hierarchy		:: -
E- Design Resources		
- 🔛 .\jsl28114_an1613.dsn		
E-2 SOLEMATICI		
PAGE1	P	
Library		111
- Outputs		111
F - PSpice Resources		111
		111
		111
		111
	1	
	•	
		111 -
	•	► //:

FIGURE 22. SIMULATION SCHEMATIC PAGE

Before we can place the new sub-circuit model and run a simulation, we need to set-up the simulation profile and add the library. Click on PSpice in the tool bar and select New Simulation Profile. Figure 23 will appear. Then type in any name that will help you keep track of the different simulations. Then click Create and Figure 24 will appear.

New Simulation	×
Name:	Create
AC Analysis	Cicdic
	Cancel
Inherit From:	
none 💌 .	
Root Schematic: SCHEMATIC1	

FIGURE 23. NAMING SIMULATION PROFILE

Click the Configuration Files tab. Then click on Library in the Category field (highlighted in blue). Browse to where to saved the Library file. Then click the Add to Design button. The Simulation Settings screen should look like that shown in Figure 24 with the file path name being the location of the common directory. Click the Apply button.

Simulation Settin	gs - AC Analysis Configuration Files Options Data Collection Probe Window
Category: Stimulus Library Include	Details Details Filename: V4ppnotes/4N1613/SPICE Model Folder/ISL28114.ib Browse Configured Files Image: Imag
	Http://www.andline.com/an
	Library Path "C:\Cadence\SPB_16.2\tools\pspice\library" Browse
	OK Cancel Apply Help

FIGURE 24. CONFIGURATION FILE TO ADD LIBRARY

Now click the analysis tab and configure the simulation as shown in Figure 25. The analysis selected for this example is an AC Sweep/Noise. Other types of analysis are: Time Domain (Transient), DC Sweep and Bias Point. Just click the down arrow in the analysis type section to access the different Analysis options. When done, click OK.

AC Sweep/Noise C Linear Start Frequency: 0.1 C Dptions: C General Settings Decade Points/Decade: 100 Noise Analysis No	General Analysis Configuration Analysis type:	n Files Options Data Col	lection Probe Window	_
Options:	AC Sweep/Noise 🗨	C Linear	Start Frequency: 0,1	
Output Cato/Worst Case Parametric Sweep Save Bias Point Load Bias Point Output Voltage: Intervel: Output File Options Therevel:	Options:	Content Logarithmic	End Frequency: 100Meg	
Emabled Output Voltage: Interval: Output File Options Include detailed bias point information for nonlinear	Monte Carlo/Worst Case	,	Points/Decade: 100	
Output File Options	Save Bias Point	Enabled Out		
Include detailed bias point information for nonlinear		Inte	rval:	

FIGURE 25. SCREEN TO SET-UP THE ANALYSIS PROFILE CONFIGURED

The user will need to add the Library .olb to the simulator. To do this, click on Place in the tool bar and select Part. This will bring up the part placement tool at the far right of the simulator as shown in Figure 26.

Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that the Application Note or Technical Brief is current before proceeding.

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To add the library, click on the tab where the arrow is pointing to in Figure 26.

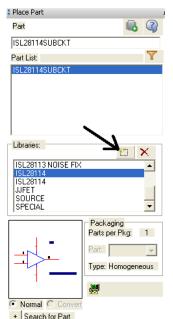


FIGURE 26. PART PLACEMENT TOOL

This will bring up the screen shown in Figure 27. Browse to where you saved the Netlist in the common directory and click Open.

Browse File						? ×
Look in	C SPICE Mode	l Folder	•	G 🦻	بي 🥲	
My Recent Documents Desktop My Documents My Computer: My Computer: NBK80JBPH1	DISL28114_AN	1613-PSpiceFiles				
S	File name:	ISL28114.0LB			•	Open
My Network Places	Files of type:	Capture Library(*.olb)			•	Cancel
Fraces		🔲 Open as read-only				

FIGURE 27. CONNECTING THE SYMBOL LIBRARY TO SIMULATOR

Now you are ready to add the sub-circuit to your simulation schematic and start your simulations.

Adding the Sub-circuit to Your Simulation Schematic

With the .lib file added to the simulation profile and the .olb file added to the Part placement tool, your are now ready to place the Opamp sub-circuit into your simulation schematic. Figure 28 shows the part placement tool after the .olb has been added to it. Under the Libraries section, find the new .olb symbol you added in the previous step (highlighted in blue). Double click on the file to add the sub-circuit to the Part list section (also highlighted in blue). Double click on the Part in the part list section to add the sub-circuit to the simulation schematic.

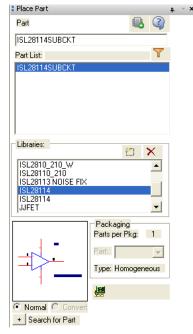


FIGURE 28. ADDING SUB-CIRCUIT TO SIMULATION SCHEMATIC

Figure 29 shows sub-circuit in a basic non-inverting application circuit. The simulation result showing AVOL (green trace) and Phase (pink) are shown in Figure 30.

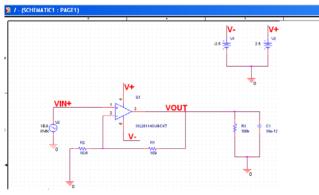


FIGURE 29. SIMULATION SCHEMATIC



FIGURE 30. AVOL GAIN/PHASE SIMULATION RESULTS